DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAF-8300CE Image Sensor

3326 (H) x 2504 (V)
Full-Frame CCD Color Image Sensor
With Square Pixels for Color Cameras

April 18, 2005
Revision 1.1

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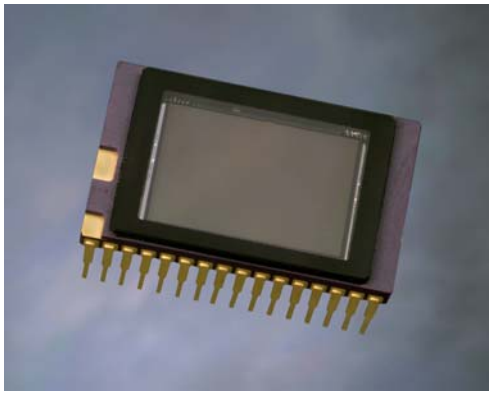
SUMMARY SPECIFICATION

KODAK KAF-8300 Image Sensor 3326 (H) x 2504 (V) Full-Frame CCD Color Image Sensor



Description

The KAF-8300CE is a 22.5mm diagonal (Type 4/3) high performance color full-frame CCD (charge-coupled device) image sensor designed for a wide range of color image sensing applications including digital imaging. Each pixel contains blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 5.4µm square pixels are patterned with an RGB mosaic color filter with overlying microlenses for improved color response and reproduction. A border of buffer and light-shielded pixels surrounds the photoactive pixels.

This device is manufactured in Rochester, NY by The Eastman Kodak Company – Image Sensor Solutions.

All parameters above are specified at T = 60°C and a data rate of 28MHz.

REVISION NO.: 1.1B
EFFECTIVE DATE: March xx, 2005

Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	3448 (H) x 2574 (V) = approx. 8.90M
Number of Effective Pixels	3358 (H) x 2536 (V) = approx. 8.6M
Number of Active Pixels	3326 (H) x 2504 (V) = approx. 8.3M
Pixel Size	5.4µm (H) x 5.4µm (V)
Imager Size	22.5mm (diagonal)
Chip Size	19.7mm (H) x 15.04mm (V)
Aspect Ratio	4:3
Saturation Signal	25.5 K e^-
Charge to Voltage Conversion	23 uV/e-
Quantum Efficiency (RGB)	0.32, 0.40, 0.32
Total Sensor Noise	16 e^-
Dark Signal	200 e-/s
Dark Current Doubling Temperature	5.8 ºC
Linear Dynamic Range	64.0 dB
Linearity Error at 12ºC	+/- 8%
Charge Transfer Efficiency	0.99999
Blooming Protection @1ms integration time	1000x saturation exposure
Maximum Data Rate	28 MHz
Package	32-pin CerDIP, 0.070” pin spacing
Cover Glass	Clear with shadow mask

DEVICE DESCRIPTION

Architecture

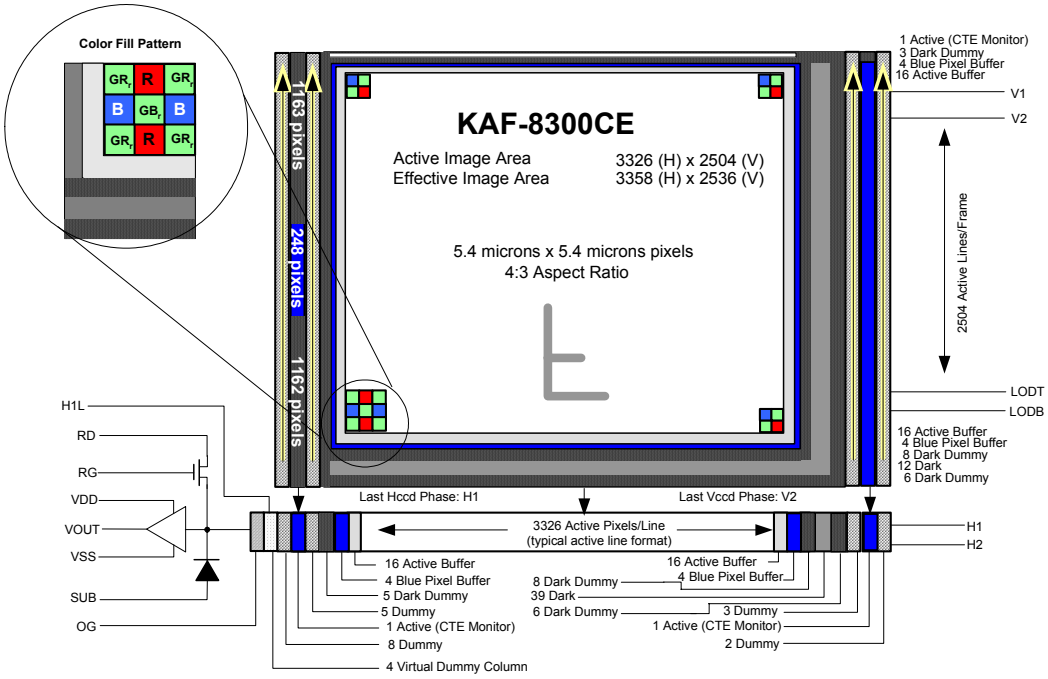


Figure 1 - Sensor Architecture

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 39 trailing dark pixels on every line. There are also 12 full dark lines at the start of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

Dark Dummy Pixels

Within the dark region some pixels are in close proximity to an active pixel, or the light sensitive regions that have been added for manufacturing test purposes, (*CTE Monitor*). In both cases, these pixels can scavenge signal depending on light intensity and wavelength. These pixels should not be used as a dark reference. These pixels are called *dark dummy pixels*.

Within the dark region, dark dummy pixels have been identified. There are 5 leading and 14 (6 + 8) trailing dark pixels on every line. There are also 14 (6 + 8) dark dummy lines at the start of every frame along with 3 dark dummy lines at the end of each frame.

Dummy Pixels

Within the horizontal shift register there are 13, (8 + 5), leading and 5, (2 + 3), trailing additional shift phases that are not electrically associated with any columns of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as *dummy pixels*. For this reason, they should not be used to determine a dark reference level.

Virtual Dummy Columns

Within the horizontal shift register there is 4 leading shift phases that are not physically associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as *virtual dummy columns*. For this reason, they also should not be used to determine a dark reference level.

Active Buffer Pixels

Sixteen buffer pixels adjacent to the blue pixel buffer regions contain a RGB mosaic color pattern. This region is classified as *active buffer pixels*. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

Blue Pixel Buffer

Four buffer pixels adjacent to any leading or trailing dark reference regions contain a blue filter. This region is classified as a *blue pixel buffer*. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

CTE Monitor Pixels

Within the horizontal dummy pixel region two light sensitive test pixels (one each on the leading and trailing ends) are added and within the vertical dummy pixel region one light sensitive test pixel has been added. These *CTE monitor pixels* are used for manufacturing test purposes. In order to facilitate measuring the device CTE, the pixels in the CTE Monitor region in the horizontal and vertical portion is coated with blue pigment.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion. On each falling edge of H1 a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

Horizontal Register

Output Structure

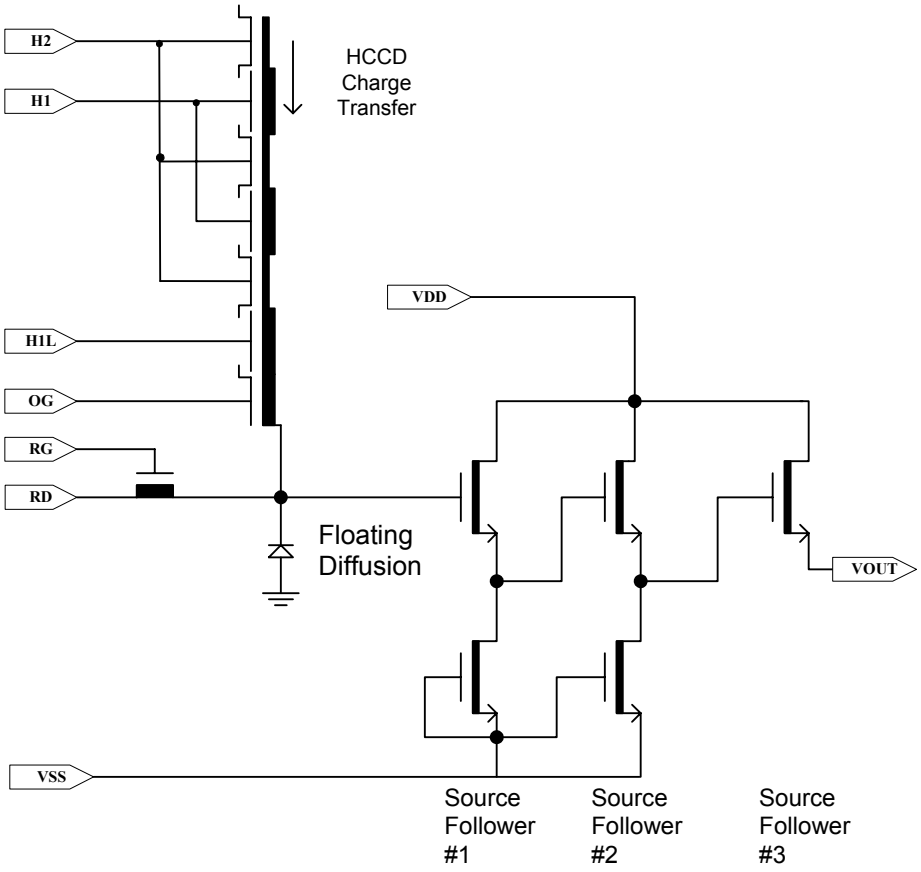


Figure 2 - Output Architecture

Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is

clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip load must be added to the VOUT pin of the device. See Figure 3.

Output Load

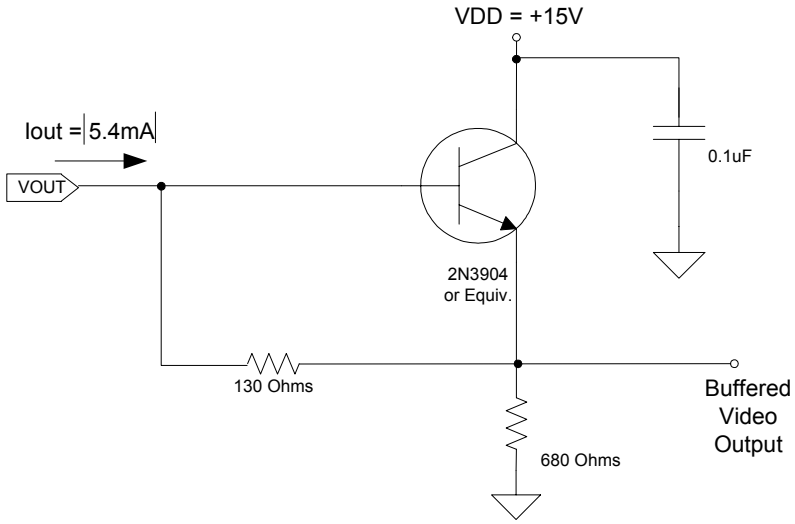
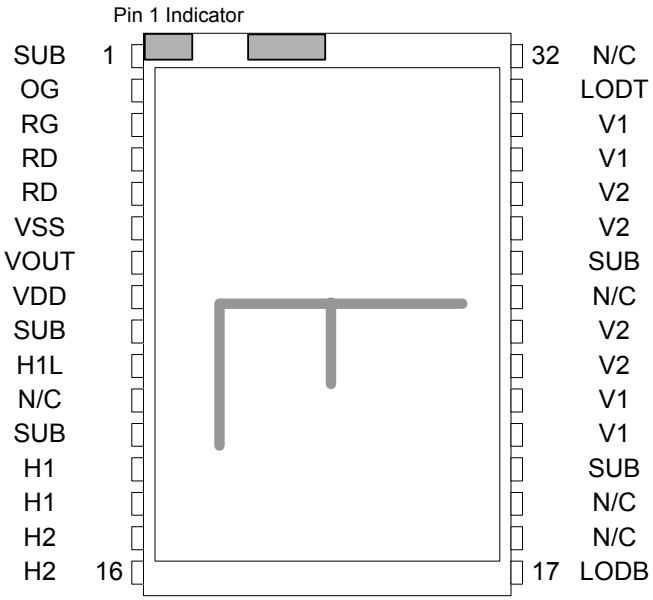


Figure 3 – Recommended Output Structure Load Diagram

Component values may be revised based on operating conditions and other design considerations.

Physical Description

Pin Description and Device Orientation



Pin	Name	Description	Pin	Name	Description
1	SUB	Substrate	32	N/C	No Connection
2	OG	Output Gate	31	LODT	Lateral Overflow Drain Top
3	RG	Reset Gate	30	V1	Vertical Phase 1
4	RD	Reset Drain Bias	29	V1	Vertical Phase 1
5	RD	Reset Drain Bias	28	V2	Vertical Phase 2
6	VSS	Output Amplifier Return	27	V2	Vertical Phase 2
7	VOUT	Output	26	SUB	Substrate
8	VDD	Output Amplifier Supply	25	N/C	No Connection
9	SUB	Substrate	24	V2	Vertical Phase 2
10	H1L	Horizontal Phase 1, Last Gate	23	V2	Vertical Phase 2
11	N/C	No Connection	22	V1	Vertical Phase 1
12	SUB	Substrate	21	V1	Vertical Phase 1
13	H1	Horizontal Phase 1	20	SUB	Substrate
14	H1	Horizontal Phase 1	19	N/C	No Connection
15	H2	Horizontal Phase 2	18	N/C	No Connection
16	H2	Horizontal Phase 2	17	LODB	Lateral Overflow Drain Bottom

Note:
Wherever possible, all N/C pins (11, 18, 19, 25, 32) should be connected to GND (0V).

Figure 4 – Package Pin Description

PERFORMANCE

Image Performance Operational Conditions

Description	Condition - Unless otherwise noted	Notes
Readout Time ($t_{readout}$)	370.36 msec	Includes $t_{Voverclock}$ & $t_{Hoverclock}$
Integration time (t_{int})	33 msec	
Horizontal clock frequency	28 MHz	
Mode	Flush – integrate – readout cycle	

Imaging Performance Specifications

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan[18]
Minimum Column	MinColumn	574			mV	1	die
Linear Saturation Signal	Ne^-_{sat}	25.5K			e^-	1,3	design
Charge to Voltage Conversion	Q-V	22.5	23		µV/e^-		design
Sensitivity							
red,	Rresp	260		420	mV		die
green,	Gresp	442		638	mV		die
blue	Bresp	230		420	mV		die
Off-band Response							
Green inband,	**Gr_Gresp**	362		630	mV		die
Red response	Gr_Rresp	0		130	mV		die
Blue response	Gr_Bresp	0		260	mV		die
Red inband,	**Rd_Rresp**	180		430	mV		die
Green response	Rd_Gresp	0		120	mV		die
Blue response	Rd_Bresp	0		45	mV		die
Blue inband,	**Bl_Bresp**	90		420	mV		die
Red response	Bl_Rresp	0		40	mV		die
Green response	Bl_Gresp	0		120	mV		die

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan[18]
Linearity Error	LeLow10	-10		10	%	2,5,6	die
	LeLow33	-10		10	%	2,5,6	die
	LeHigh	-10		10	%	2,5	die
Linearity Balance	Red_Bal	-14	6.4	14	%	2, 6	die
	Blu_Bal	-8	0.2	8	%	2, 6	die
Photo Response Non-Uniformity	R_PRNU			15	%p-p	7	die
	G_PRNU			15	%p-p	7	die
	B_PRNU			15	%p-p	7	die
High Frequency Noise	R_Nois			2	%rms		die
	GRr_Nois			2	%rms		die
	GBr_Nois			2	%rms		die
	B_Nois			2	%rms		die
Dark Signal (Active Area Pixels)	AA_DarkSig			200	e-/s	8	die
Dark Signal (Dark Reference Pixels)	DR_DarkSig			200	e-/s	8	die
Readout Cycle Dark Signal	Dark_Read			15	mV/s		die
Flush Cycle Dark Signal	Dark_Flush		43	90	mV/s		die
Dark Signal Non-Uniformity	DSNU		1.30	3	mVp-p	9	die
	DSNU_Step		0.14	0.5	mV p-p	9	die
	DSNU_H		0.4	1.0	mVp-p	9	die
Dark Signal Doubling Temperature	ΔT		5.8		°C		design
Dark Reference Difference, Active Area	DarkStep	-3.5	0.15	3.5	mV		die
Total Noise	Dfld_noi			1.08	mV	10	die
Total Sensor Noise	N		16		e^- rms	19	design
Linear Dynamic Range	DR		64.0		dB	11	design
Red-Green Hue Shift	RGHueUnif			10	%	12	die
Blue-Green Hue Shift	BGHueUnif			12	%	12	die
GRr/GBr Hue Uniformity	GrGbHueUnf			7	%	12	die
Green Light GRr/GBr Hue Uniformity	Gr_GHueUnf			9	%		die
Low Hue Uniformity	RGLoHueUnf			12	%		die
	BGLoHueUnf			10	%		die
Streak/Spot	GrnStreak			40	%		
	RedStreak			20	%		
	BluStreak			20	%		

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan[18]
Horizontal Charge Transfer Efficiency	HCTE	0.999990	0.999995			13, 21	die
Vertical Charge Transfer Efficiency	VCTE	0.99997	0.999999		%	21	die
Blooming Protection	X_b	1000			x Esat	14	design
Vertical Bloom on Transfer	VBloomF	-20		20	mV		die
Horizontal Crosstalk	H_Xtalk	-20		20	mV		die
Horizontal Overclock Noise	Hoclk_noi	0		1.08	mV		die
Output Amplifier Bandwidth	f_{-3dB}	88		159	Mhz	6,16	die
Output Impedence, Amplifier	R_{OUT}	100		180	Ohms		die
Hclk Feedthru	V_{hft}			70	mV	17	die
Reset Feedthru	V_{rft}	500	710	1000	mV		design
Local Green Difference							
white light, min	W_GNU_Min			4	%		die
white light, max	W_GNU_Max			6	%		die
green light, min	Gr_GNU_Min			4	%		die
green light, max	Gr_GNU_Max			4	%		die
red light, min	R_GNU_Min			65	%		die
red light, max	R_GNU_Max			65	%		die
blue light, min	B_GNU_Min			40	%		die
blue light, max	B_GNU_Max			40	%		die
Chroma Test	UL_Chroma			7	%		die
	UR_Chroma			7	%		die
	LL_Chroma			7	%		die
	LR_Chroma			7	%		die
Hue Test	UL_UR_Hue			6	%		die
	UL_LR_Hue			6	%		die
	UL_LL_Hue			6	%		die
	UR_LR_Hue			6	%		die
	UR_LL_Hue			6	%		die
	LR_LL_Hue			6	%		die

Notes:
1. Increasing output load currents to improve bandwidth will decrease these values.
2. Specified from 12ºC to 60ºC.
3. Saturation signal level achieved while meeting Le specification. Specified from 0ºC to 40ºC.
4. This note left blank.

5. Worst case deviation, (from 10mV to Vsat min), relative to a linear fit applied between 0 and 500mV exposure.
6. Tested at T=25ºC.
7. Peak to peak non-uniformity test based on an average of 185 x 185 blocks.
8. Average non-illuminated signal with respect to over clocked horizontal register signal.
9. Absolute difference between the maximum and minimum average signal levels of 185 x 185 blocks within the sensor.
10. Dark rms deviation of a multi-sampled pixel as measured using the KAF-8300CE Evaluation Board.
11. 20log(Vsat/N)
12. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest of 185 x 185 blocks.
13. Measured per transfer at 80% of Vsat.
14. Esat equals the exposure required to achieve saturation. X_b represents the number of Esat exposures the sensor can tolerate before failure. X_b characterized at 25 °C.
15. Video level DC offset with respect to ground at clamp position. Refer to Pixel Timing Diagram Figure 11.
16. Last stage only. CLOAD = 10pF. Then f_{-3dB} = (1 / (2π*ROUT*CLOAD)).
17. Amount of artificial signal due to H1 coupling.
18. Sampling plan defined as “die” indicates that every device is verified against the specified performance limits. Sampling plan defined as “design” indicates a sampled test or characterization, at the discretion of Kodak, against the specified performance limits.
19. Calculated value subtracting the noise contribution from the KAF-8300CE Evaluation Board.
20. Process optimization has effectively eliminated vertical striations.
21. CTE = 1 - CTI. Where CTE is charge transfer *efficiency* and CTI is charge transfer *inefficiency*. CTI is the measured value.

Typical Performance Curves

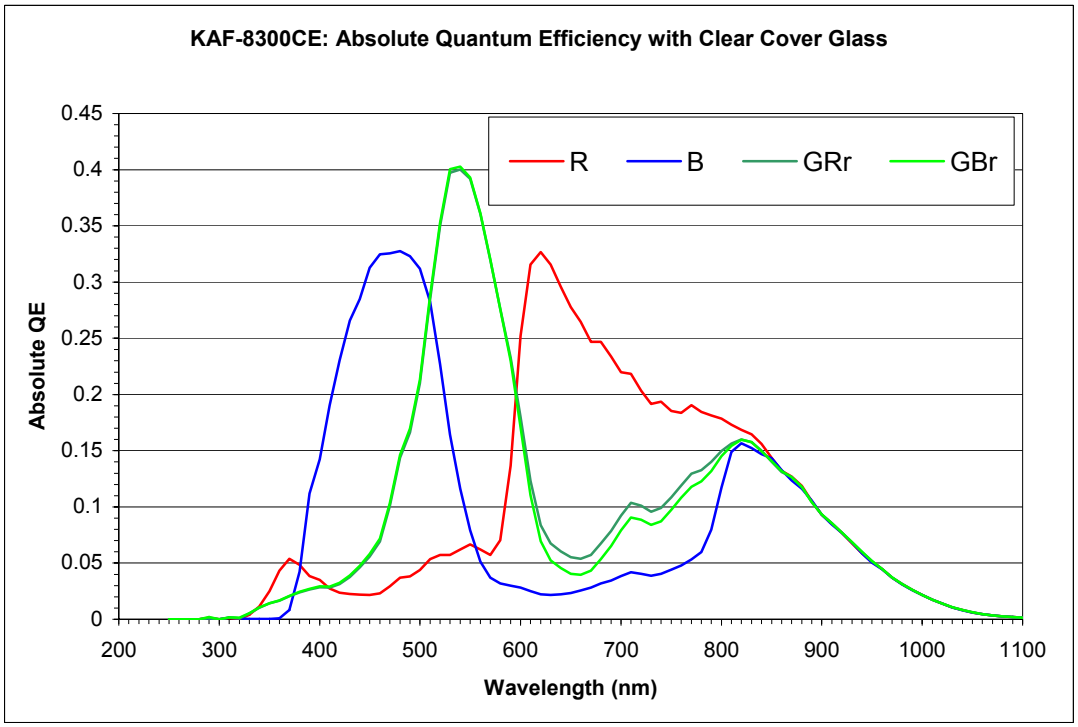


Figure 5 – Typical Quantum Efficiency

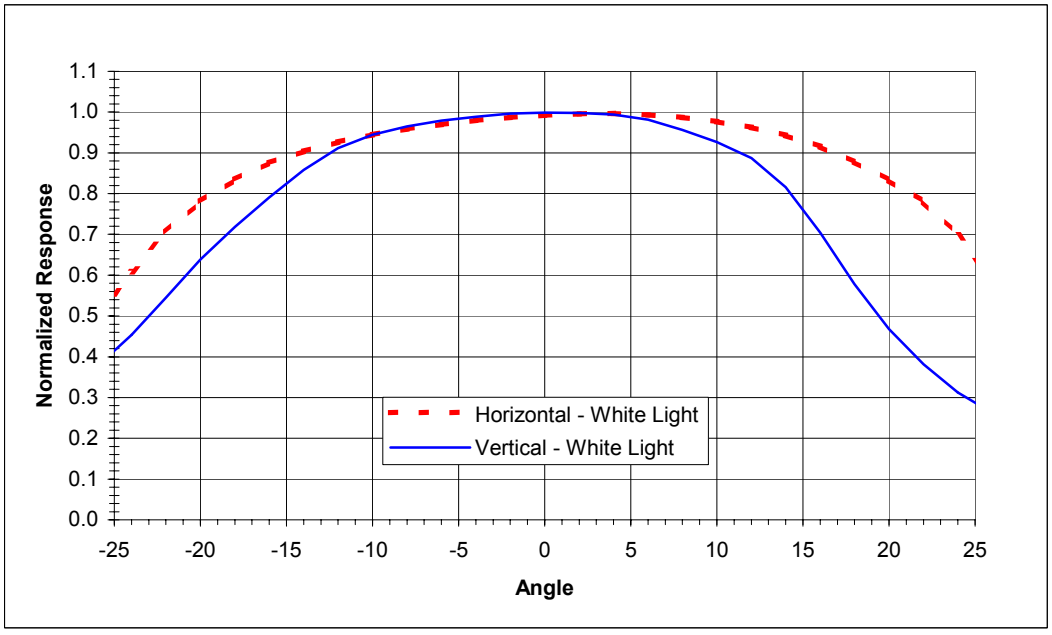


Figure 6 – Typical Angular Response – Clear Cover Glass and White Light Illumination

(Center location of die as shown.)

Defect Definitions

Defect Operational Conditions

The Defect Specifications are measured using the following conditions:

Description	Test Condition	Notes
Integration time (t_{int})	33 msec	Unless otherwise noted

Defect Specifications

Description	Symbol	Definition	Threshold	Maximum Number Allowed
Point defect	BPnt33_7	Dark field, minor, short integration time	7.5 mV	800 total (6.5.1 Total_Pnts)
Point defect	Bfld_Pnt_D	Dark point in an illuminated field	11%	
Point defect	Bfld_Pnt_B	Bright point in an illuminated field	7%	
Point defect	BPnt33_100	Dark field, major, short integration time	100 mV	
Point defect	BPnt33_500	Dark field, major, short integration time	500 mV	0
Point defect	BPnt333_13	Dark field, minor, long integration time, t_{int}=1/3 sec	13 mV	32,500[1]
Point Defect	DR_BPnts	Bright point in the dark reference region	7.5 mV	0
Cluster defect	Total_Clst	A cluster is a group of 2 or more defective pixels that do not exceed the perpendicular pattern defect.		6 total
Cluster defect	Dfld_VPerp	Dark field very long exposure bright cluster where 9 or more adjacent point defects exist, very long integration time, t_{int}=1 sec	3.04 mV	0
Cluster Defect – Perpendicular Pattern Defect	Dfld_Perp Bfld_Perp Total_Perp	Three or more adjacent point defects in the same color plane, along a row or column. [2]		0
Column defect, illuminated	Bfld_Col_D Bfld_Col_B	A column which deviates above or below neighboring columns under illuminated conditions (>300mV signal) greater than the threshold	1.5% 1.5%	0

Description	Symbol	Definition	Threshold	Maximum Number Allowed
Column defect, darkfield	Dfld_Col2 Dfld_Col4 Lo_Col_B Lo_Col_D Lo_Col_B1 Lo_Col_D1	A column which deviates above or below neighboring columns under non-illuminated or low light level conditions (~10mV) greater than the threshold	1 mV 1 mV 1 mV 1 mV 1 mV 1 mV	0
Row Defect	Dfld_Row	Row defect if row average deviates above threshold	1 mV	0
Streak Test, color	GrnStreak RedStreak BluStreak	Maximum defect density gradient allowed in a color bit plane.[4]	40% 20% 20%	0
Streak Test, dark	DarkStreak	Maximum defect density gradient allowed in the entire imaging area.[5]	40%	0
LOD Bright Col, dark	Dfld_LodCol	Defines functionality and uniform efficiency of LOD structure	1.5 mV	0

Notes:
1. This parameter is only a quality metric and these points will not be considered for cluster and point criteria.
2. Green pixels in a red row (GR) are considered a different color plane than the green pixels in a blue row (GB).
3. This note left blank.
4. As the gradient threshold is defined as 8.5 mV maximum across a 16 x 16 pixel region about each pixel.
5. As the gradient threshold is defined as 6 mV maximum across a 50 x 50 pixel region about each pixel.

OPERATION

Absolute Maximum Ratings

Description[9]	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+17.5	V	1,2
Gate Pin Voltages	V_{gate1}	-13.5	+13.5	V	1,3
Overlapping Gate Voltages	V_{1-2}	-13.5	+13.5	V	4
Non-overlapping Gate Voltages	V_{g-g}	-13.5	+13.5	V	5
V1, V2 – LOD Voltages	V_{V-L}	-13.5	+13.5	V	6
Output Bias Current	I_{out}		-30	mA	7
LODT Diode Voltage	V_{LODT}	-0.5	+13.0	V	8
LODB Diode Voltage	V_{LODB}	-0.5	+18.0	V	8
Operating Temperature	T_{OP}	-10	70	°C	10
Guaranteed Temperature of Performance	T_{SP}	0	60	°C	11

Notes:
1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2.
6. Voltage difference between V1 and V2 gates and LODT, LODB diode.
7. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
8. V1, H1, V2, H2, H1L, OG, and RD are tied to 0V.
9. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
10. Noise performance will degrade at higher temperatures.
11. See section for Imaging Performance Specifications.

Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	I_{RD} = 0.01	
Output Amplifier Return	VSS	1.05	1.25	1.45	V	I_{SS} = -3.0	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	
Substrate	SUB		GND		V	-0.01	2
Output Gate	OG	-3	-2.8	-2.6	V	0.1	
Lateral Drain	LODT, LODB	9.5	9.75	10.0	V	0.2	2
Video Output Current	I_{OUT}	-3	-5	-8	mA		1

Notes:
1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 3.
2. Maximum current expected up to saturation exposure (Esat).

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.5	-9.25	-9.0	V	76 nF	1
V1 High Level	V1H	High	2.4	2.6	2.8	V		1
V2 Low Level	V2L	Low	-9.5	-9.25	-9.0	V	81 nF	1
V2 High Level	V2H	High	2.4	2.6	2.8	V		1
RG, H1, H2, amplitude	RG_{amp} $H1_{amp}$ $H2_{amp}$	Amp	5.5	6.0	6.5	V	RG = 7 pF H1 = 224 pF H2 = 168 pF	1
H1L, amplitude	$H1L_{amp}$,	Amp	7.5	8.0	8.5	V	7 pF	1
H1 Low Level	$H1_{low}$,	Low	-4.7	-4.5	-4.3	V		1
H1L Low Level	$H1L_{low}$	Low	-6.7	-6.5	-6.3	V		
H2 Low Level	$H2_{low}$	Low	-5.2	-5	-4.8	V		
RG Low Level	RG_{low}	Low	1.8	2.0	2.2	V		1

Notes:
1. All pins draw less than 10µA DC current. Capacitance values relative to SUB (substrate).

Clock Voltage Detail Characteristics (Note 1)

Description	Symbol	Min	Nom	Max	Units	Notes
V1 High-level variation	$V1_{HH}$	-	0.50	1	V	High-level coupling
V2 High-level variation	$V2_{HL}$	-	0.28	1	V	High-level coupling
V2 Low-level variation	$V2_{LH}$	-	0.46	1	V	Low-level coupling
V1 Low-level variation	$V1_{LL}$	-	0.14	1	V	Low-level coupling
V1-V2 Cross-over	$V1_{CR}$	-2	-0.5	1	V	Referenced to ground
H1 High-level variation	$H1_{HH}$	-	0.30	1	V	
H1 High-level variation	$H1_{HL}$	-	0.07	1	V	
H1 Low-level variation	$H1_{LH}$	-	0.16	1	V	
H1 Low-level variation	$H1_{LL}$	-	0.25	1	V	
H2 High-level variation	$H2_{HH}$	-	0.40	1	V	
H2 High-level variation	$H2_{HL}$	-	0.06	1	V	
H2 Low-level variation	$H2_{LH}$	-	0.10	1	V	
H2 Low-level variation	$H2_{LL}$	-	0.27	1	V	
H1 – H2 Cross-over	$H1_{CR1}$	-3	-1.23	0	V	Rising side of H1
H1 – H2 Cross-over	$H1_{CR2}$	-3	-0.59	0	V	Falling side of H1
H1L High-level variation	$H1L_{HH}$	-	0.64	1	V	
H1L High-level variation	$H1L_{HL}$	-	0.32	1	V	
H1Llow-level variation	$H1L_{LH}$	-	0.27	1	V	
H1Llow-level variation	$H1L_{LL}$	-	0.23	1	V	
H1L – H2 Cross-over	$H1L_{CR1}$	-1	-	-3	V	Rising side of H1L
RG High-level variation	RG_{HH}	-	0.19	1	V	
RG High-level variation	RG_{HL}	-	0.20	1	V	
RG Low-level variation	RG_{LH}	-	0.11	1	V	
RG Low-level variation	RG_{LL}	-	0.30	1	V	

Notes:
1. H1, H2 clock frequency: 28MHz. The maximum and minimum values in this table are supplied for reference. The actual clock levels were measured using from the KAF-8300CE Evaluation Board. Testing against the device performance specifications is performed using the nominal values.

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			28	MHz	1, 2
V1, V2 Clock Frequency	f_V			125	kHz	2
Pixel Period (1 Count)	t_e	35.7			ns	2
H1, H2 Setup Time	t_{HS}	1			µs	
H1L – VOUT Delay	t_{HV}		3		ns	
RG – VOUT Delay	t_{RV}		1		ns	
Readout Time	$t_{readout}$	340.2			ms	4, 5
Integration Time	t_{int}					3, 4
Line Time	t_{line}	132.2			µs	4
Flush Time	t_{flush}	21.23			ms	6

Notes:
1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Integration time is user specified.
4. Longer times will degrade noise performance.
5. $t_{readout} = t_{line} * 2574$ lines.
6. See Figure 15 for a detailed description.

Clock Switching Characteristics (Note 1)

Description	Symbol	Min	Nom	Max	Units	Notes
V1 Rise Time	t_{V1r}	-	0.26	1	us	3
V2 Rise Time	t_{V2r}	-	0.55	1	us	3
V1 Fall Time	t_{V1f}	-	0.43	1	us	3
V2 Fall Time	t_{V2f}	-	0.31	1	us	3
V1 Pulse Width	t_{V1w}	5.0	-	-	us	4, 5
V2 Pulse Width	t_{V2w}	3.0	-	-	us	4, 5
H1 Rise Time	t_{H1r}	-	9.0	10	ns	3
H2 Rise Time	t_{H2r}	-	6.9	10	ns	3
H1 Fall Time	t_{H1f}	-	5.8	10	ns	3
H2 Fall Time	t_{H2f}	-	5.4	10	ns	3
H1 – H2 Pulse Width	t_{H1w}, t_{H2w}	14	18	22	ns	
H1L Rise Time	t_{H1Lr}		1.8	4	ns	3
H1L Fall Time	t_{H1Lf}		2.5	4	ns	3
H1L Pulse Width	t_{H1Lw}	14	19.0	22	ns	
RG Rise Time	t_{RGr}	-	2.0	4	ns	3
RG Fall Time	t_{RGf}	-	2.2	4	ns	3
RG Pulse Width	t_{RGw}	-	6.7	-	ns	2

Notes:
1. H1, H2 clock frequency: 28MHz. The maximum and minimum values in this table are supplied for reference. The actual clock timing was measured using from the KAF-8300CE Evaluation Board. Testing against the device performance specifications is performed using the nominal values.
2. RG should be clocked continuously.
3. Relative to the pulse width (based on 50% of high/low levels).
4. CTE will degrade above the nominal frequency.
5. Longer times will degrade noise performance.

Pin Capacitance

Parameter	Value (typical)	Units
$C_{\Phi V1}$	61	nF
$C_{\Phi V12}$	15	nF
$C_{\Phi V2}$	67	nF
$C_{\Phi H1}$	153	nF
$C_{\Phi H12}$	36	nF
$C_{\Phi H2}$	97	nF
$C_{\Phi H1L}$	7	nF
R_{H1LH1}	52	Kohms

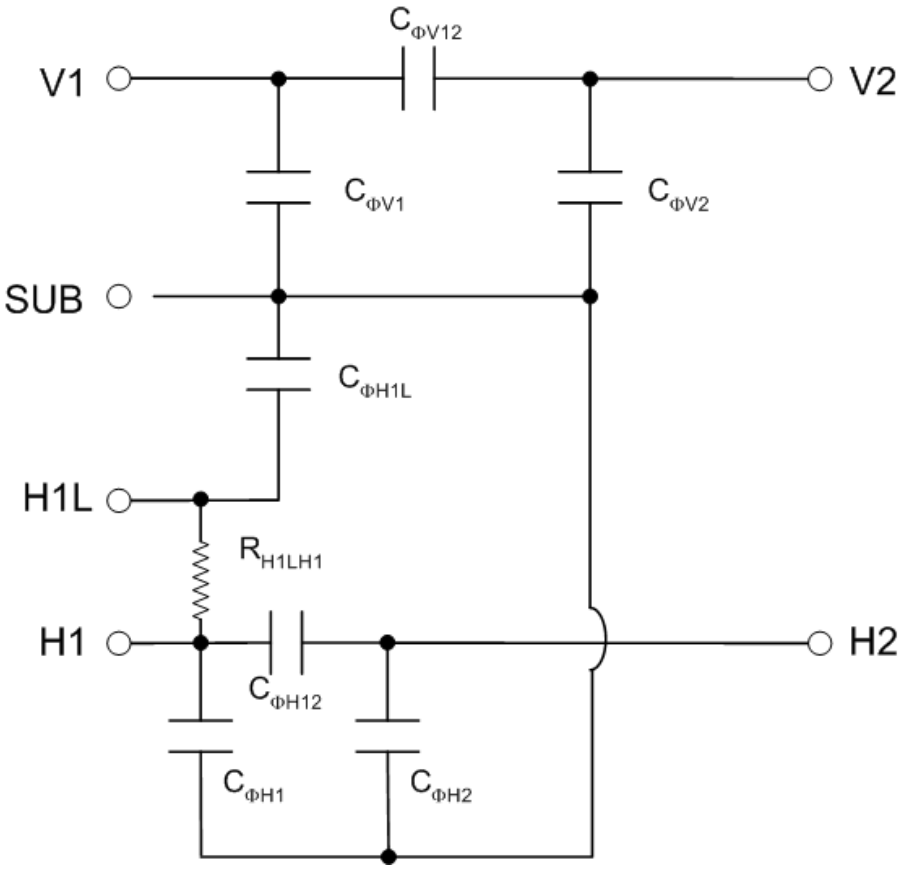


Figure 7 –Device Transfer Clock Equivalent Circuit

Frame Timing

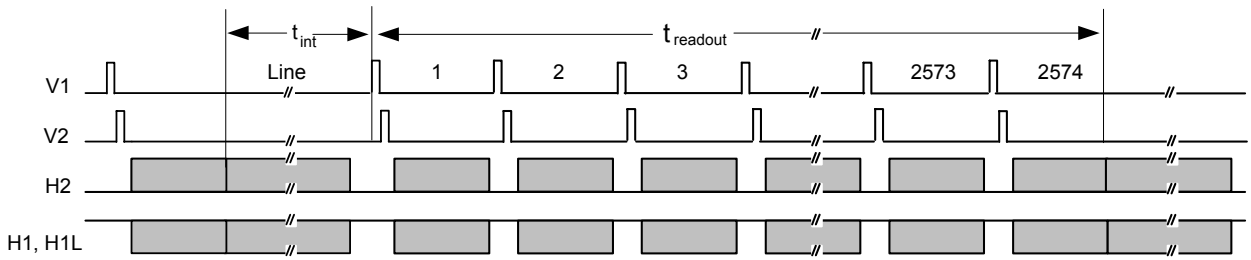


Figure 8 – Frame Timing (minimum)

Frame Timing Edge Alignment

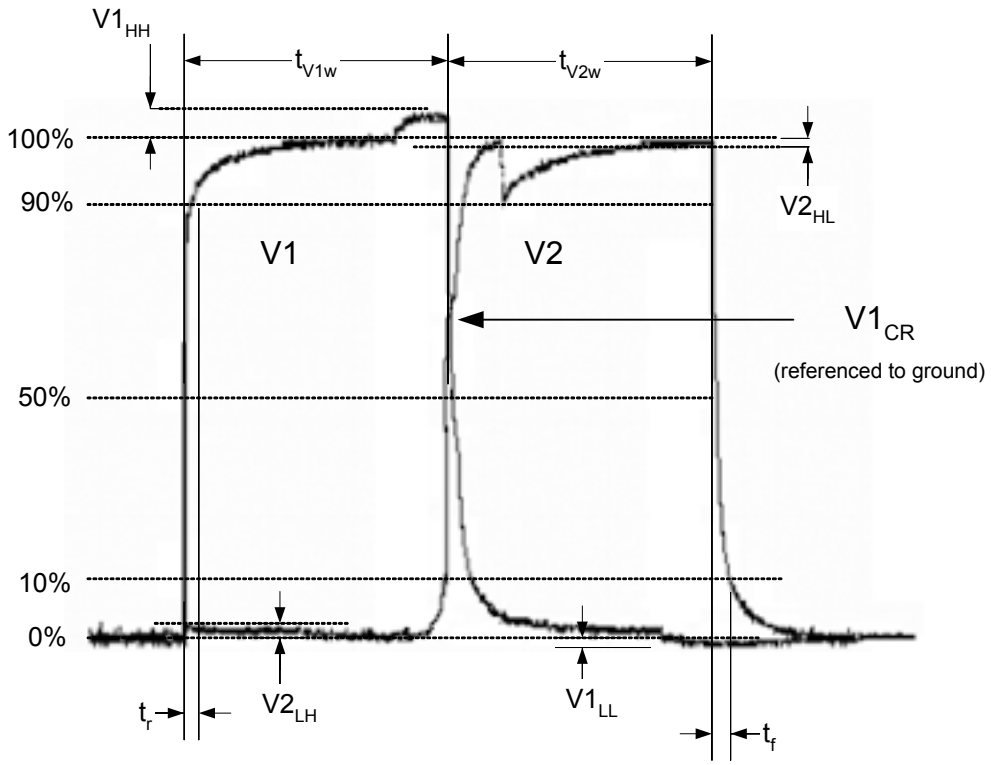


Figure 9 – Frame Timing Edge Alignment

LINE TIMING

Line Timing

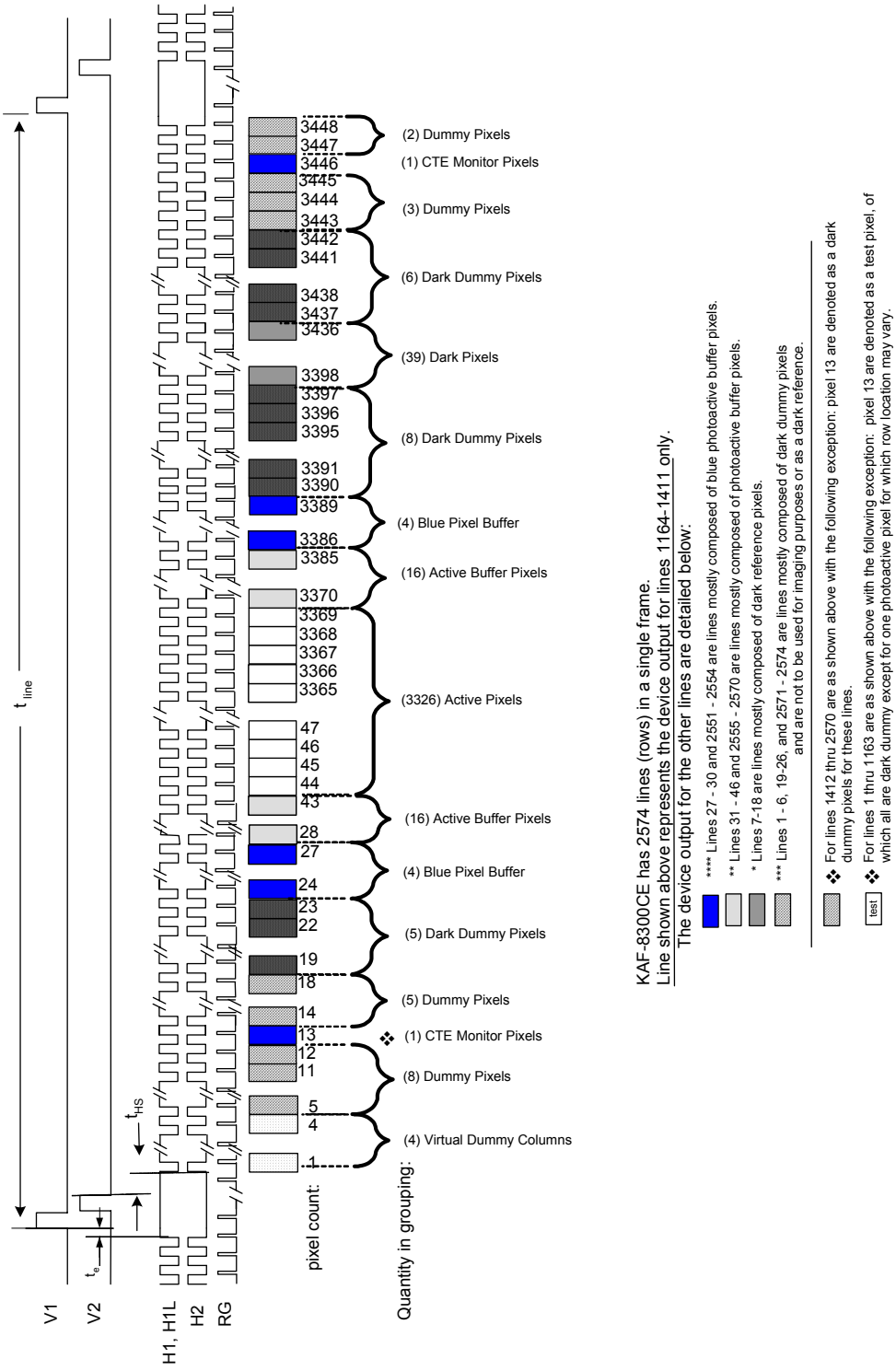


Figure 10 – Line Timing

PIXEL TIMING

Pixel Timing

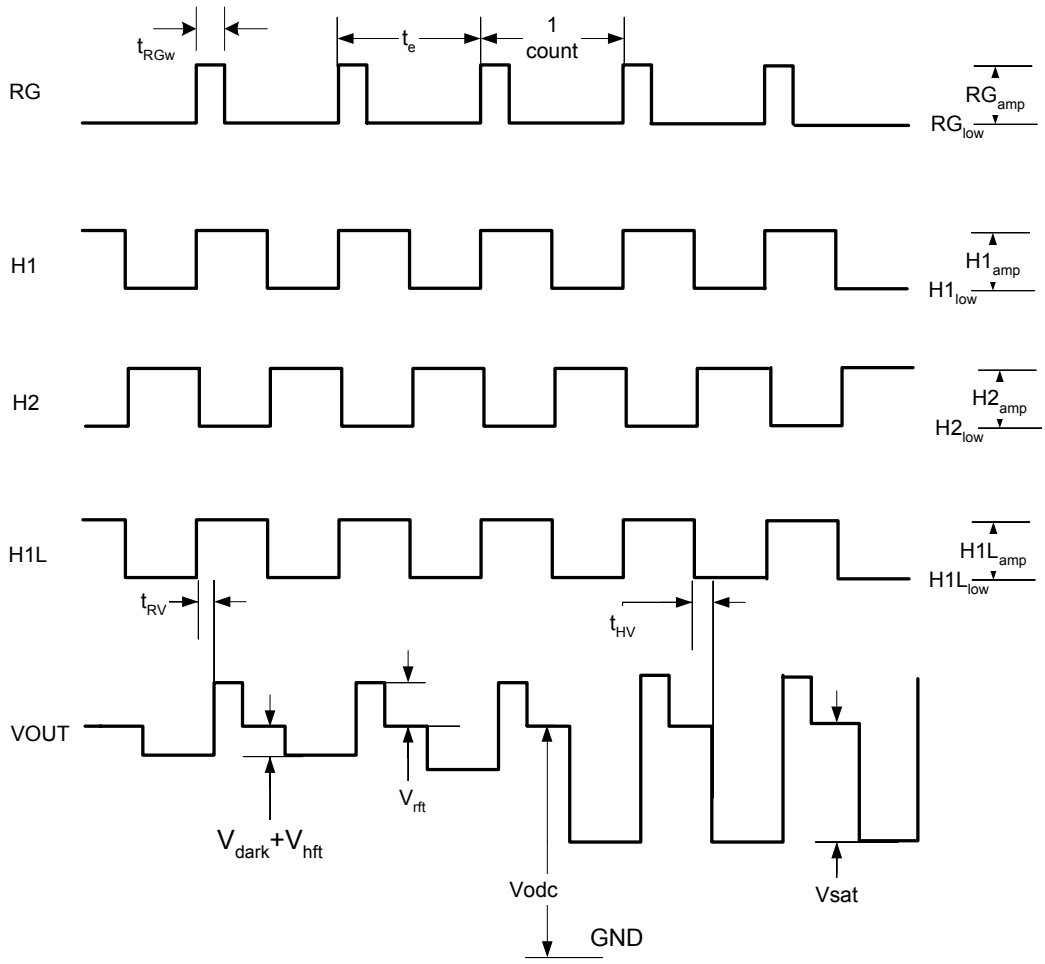


Figure 11 – Pixel Timing

Pixel Timing Detail

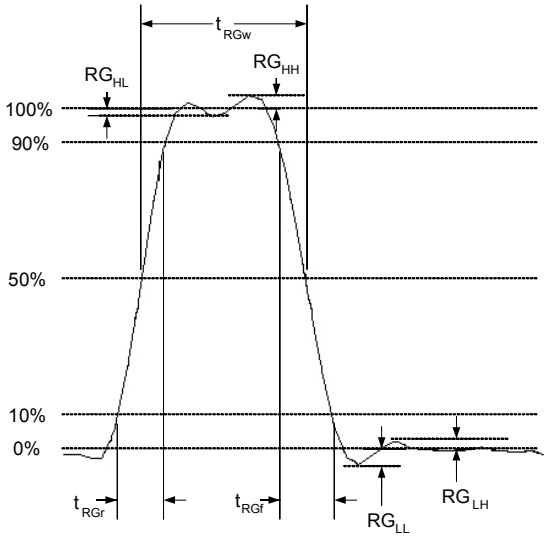


Figure 12 – Pixel Timing Detail

Pixel Timing Edge Alignment

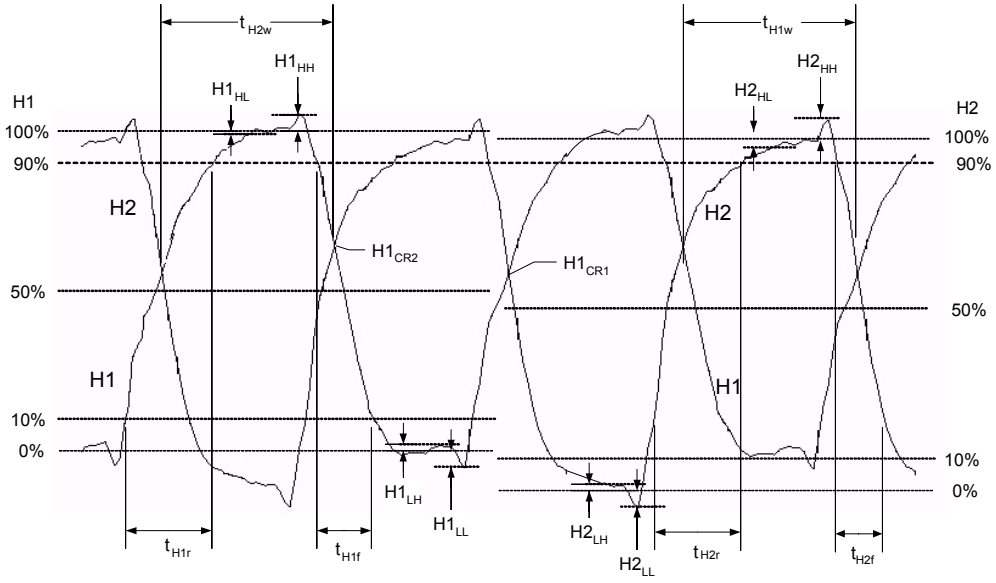


Figure 13 – H1 and H2 Edge Alignment

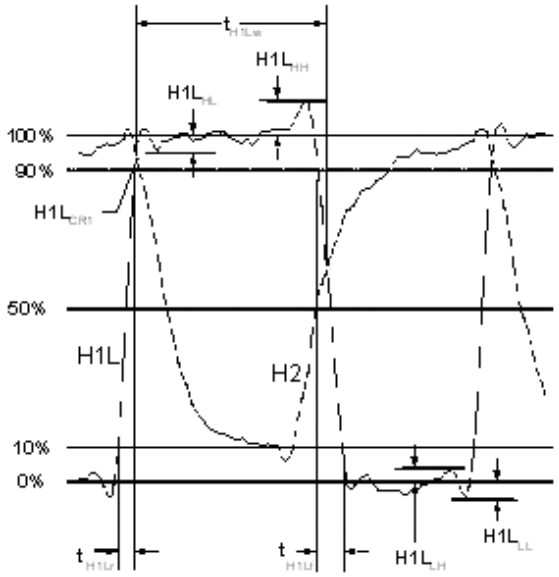


Figure 14 – H1L and H2 Edge Alignment

MODE OF OPERATION

Power-up Flush Cycle

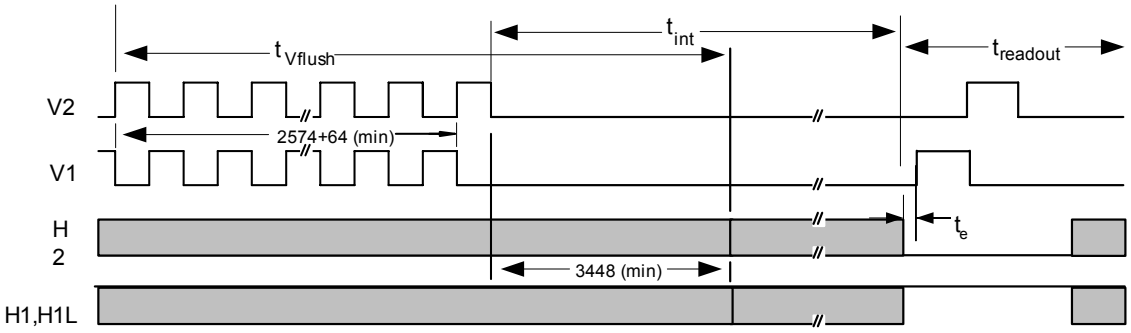


Figure 15 – Power-up Flush Cycle

STORAGE AND HANDLING

Environmental Storage Conditions

Assembled devices, in their first level packing container in a dust-free, enclosed environment with the conditions described in the table below.

Description	Symbol	Maximum	Units	Notes
Humidity	RH	60	%	1
Storage Temperature	T_{ST}	40	°C	2

Notes:
1. T=25ºC. Excessive humidity will degrade MTTF.
2. Storage toward the maximum temperature will accelerate color filter degradation.

Handling Conditions

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 2 JESD22 Human Body Model (<= 2000V) and Class B Machine Model (<=200V). Refer to Application Note MTD/PS-0224, Electrostatic Discharge Control, for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.

2. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.

Soldering recommendations

1. A typical Pb-free soldering procedure is defined as a partial heating method as follows:
   a. Using a 80 Watt ESD-safe soldering iron,
   b. 350 °C soldering iron tip temperature for less than 3 seconds per pin,
   c. Allow the part to cool to room temperature,

2. For circuit board repair, or de-soldering an image sensor, do not use solder suction equipment. In any instance, care should be given to minimize and eliminate electrostatic discharge.

Cover glass care and cleanliness

1. Devices are shipped with the cover glass region covered with a protective tape. The tape should be removed upon usage.

   Note:
   Also see section on Quality Assurance and Reliability.

Environmental Exposure

1. Do not expose to strong sun light for long periods of time. The color filters may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Color filter performance may be degraded. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.
6. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

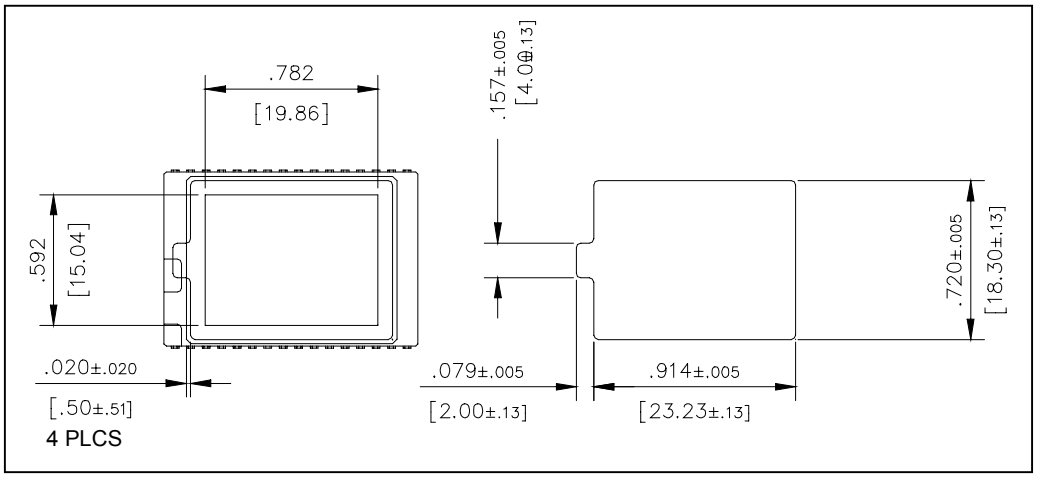


Figure 16 – Cover glass protection tape

Package Drawings

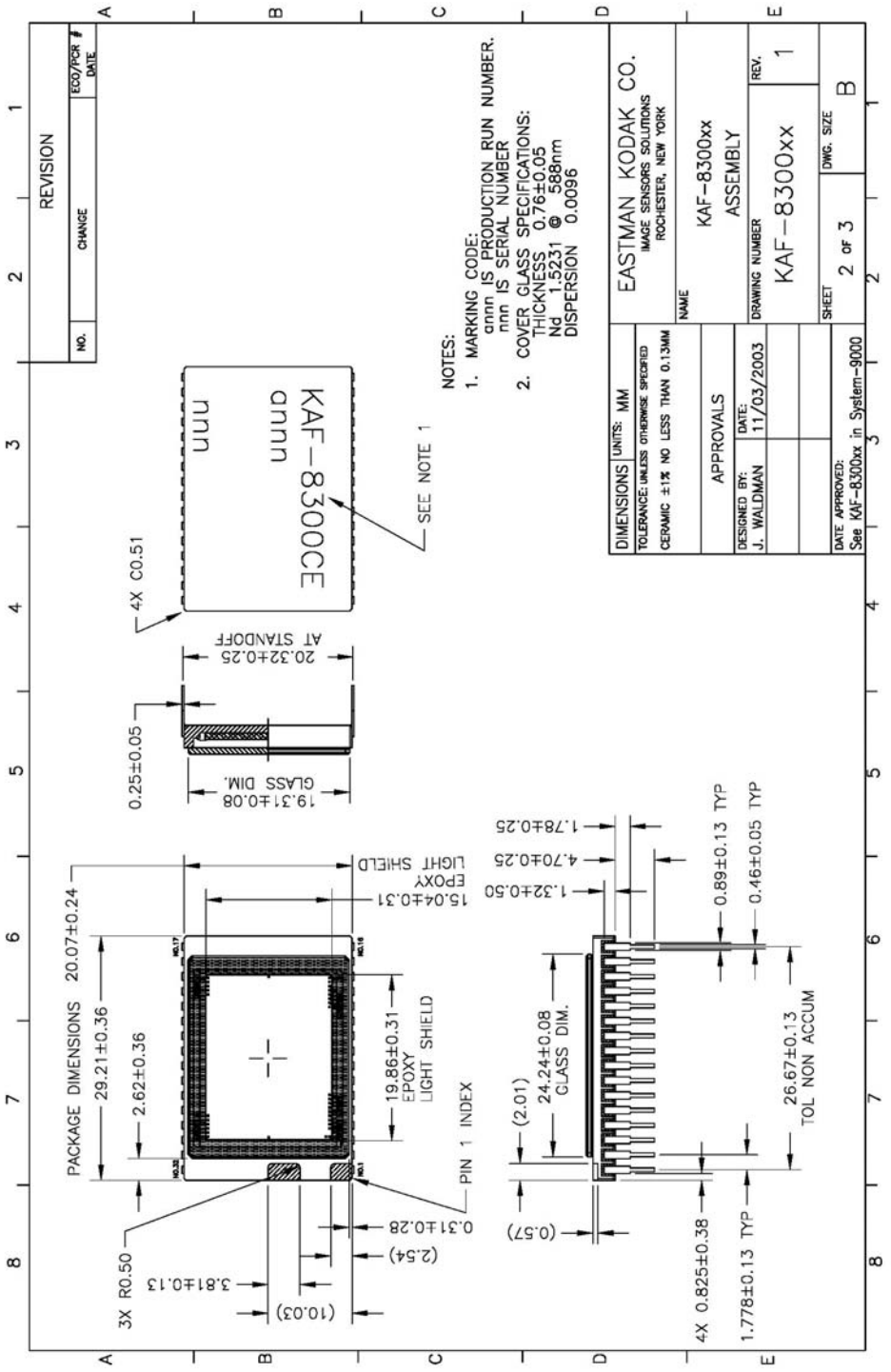


Figure 17 – Package Drawing

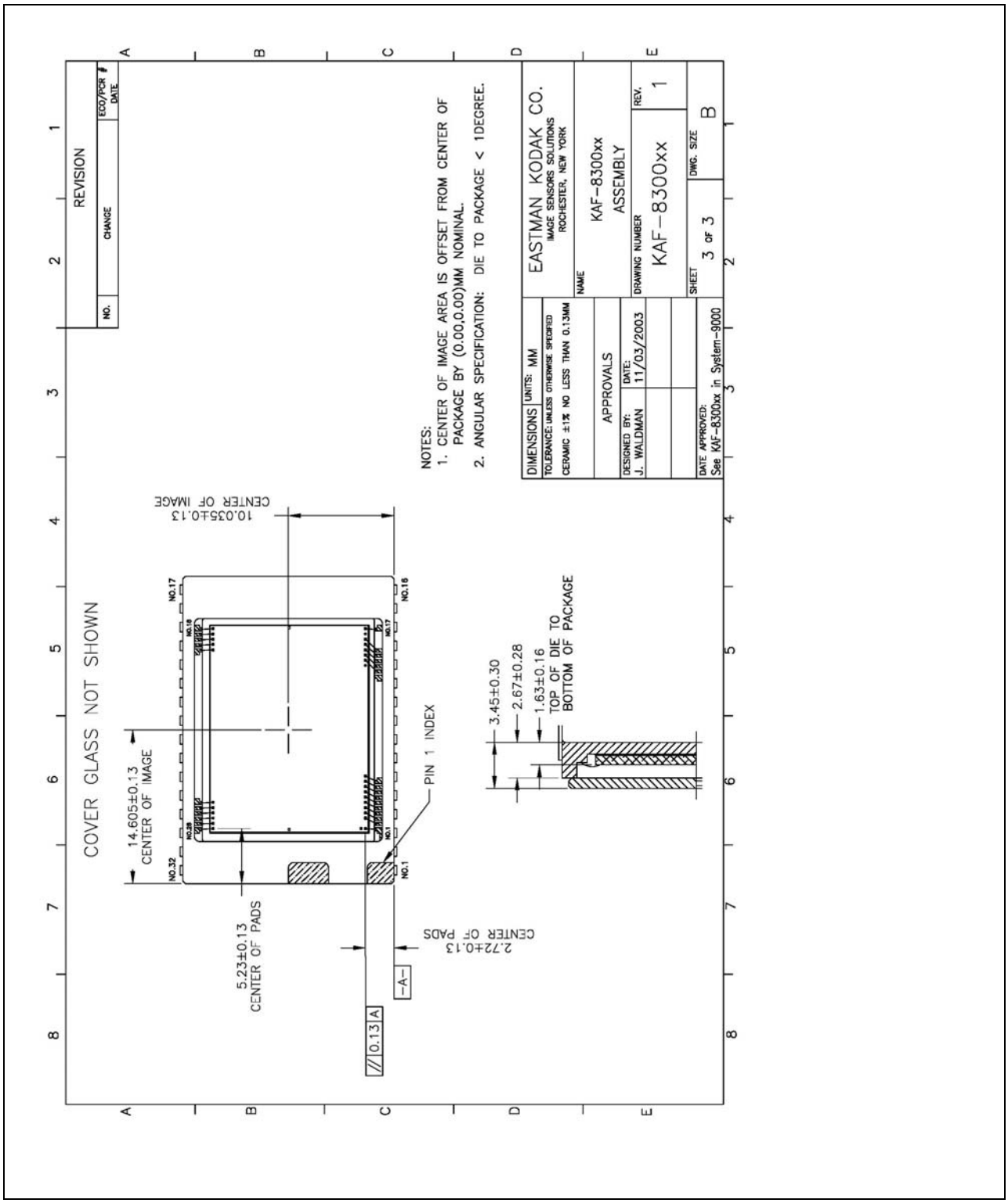


Figure 18 – Die to Package Alignment, Device Marking

Glass Transmission

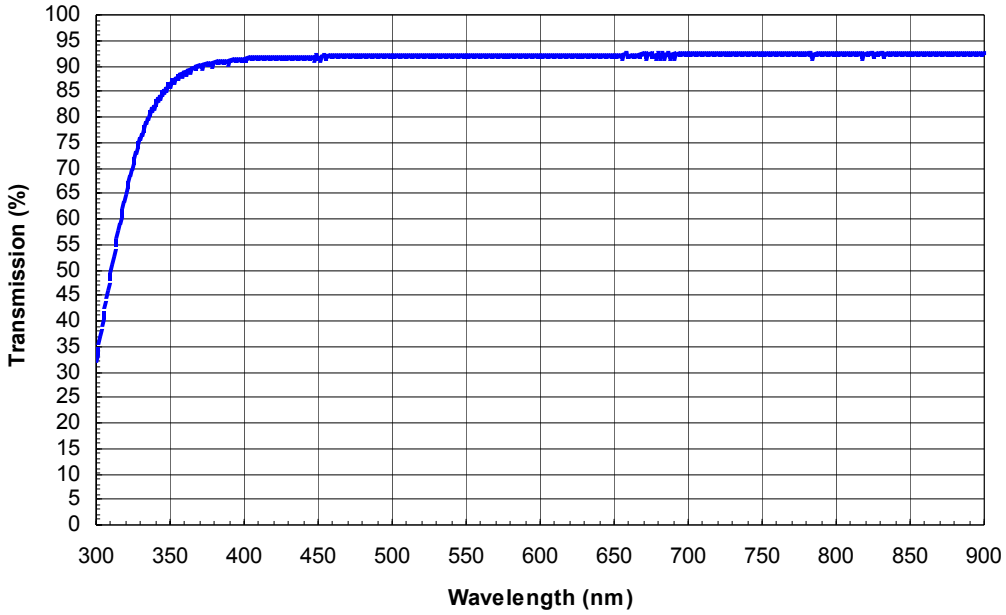


Figure 19 – Glass Transmission

Shipping Configuration

Shipping configuration is determined by order volume. Configuration shown below is for high volume shipments. Small volume shipments are packaged in individual containers.

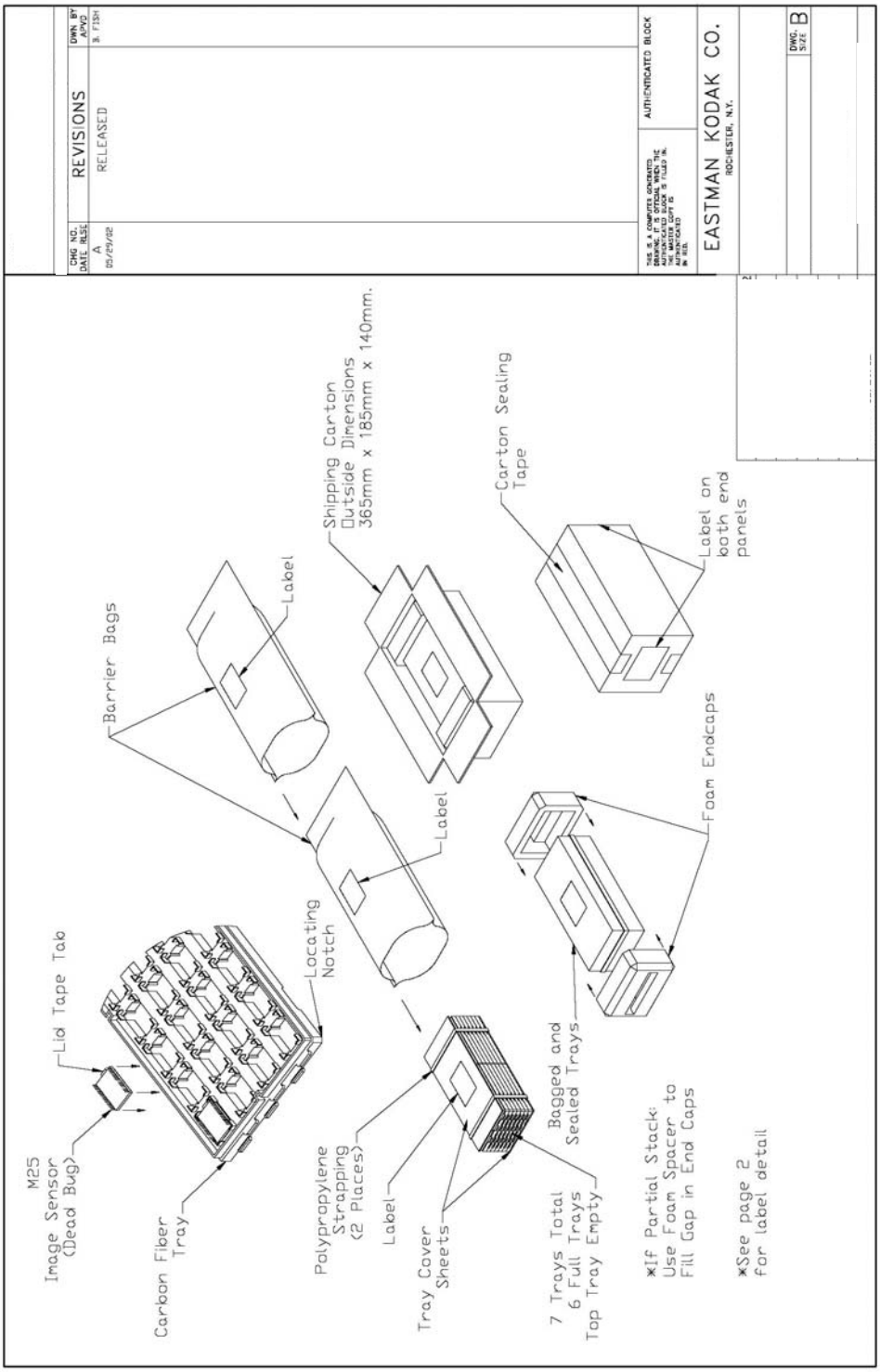


Figure 20 – Packing materials Configuration

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment. Touching the cover glass must be avoided. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237 “Cover Glass Cleaning for Image Sensors”.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224, Electrostatic Discharge Control, for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description	Glass Configuration
KAF-8300CE	4H0469 KAF8300ACELM-ANB-C Color with microlens	Clear, sealed

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone : (585) 722-4385
Fax : (585) 477-4947
E-mail : imagers@kodak.com

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1	Original version
1.1	Diode maximum rating (minimum value), Solderability and lenslets clarified. Additionally, adjusted final values for dynamic range, doubling temperature, minimum column. Corrected layout of Off-band response table on page 11.